Amendments To The Claims:

Please amend the claims as shown. Applicants reserve the right to pursue any cancelled claims at a later date.

1.-7. (canceled)

8. (new) A method for synchronizing external events supplied to a CPU, comprising:

storing the external events;

retrieving the external events in a separate operating mode of the CPU;

processing the external event by an execution unit of the CPU; and

providing a maximum number of commands to execute prior to the CPU entering the separate operating mode.

9. (new) The method as claimed in claim 8, wherein the maximum number of commands is predetermined.

10. (new) The method as claimed in claim 8, wherein the maximum number of commands is specified by a command.

11. (new) The method as claimed in claim 8, further comprising:

comparing the number of instructions executed since a change to the separate operating mode with the maximum number of commands; and

changing the CPU into the separate operating mode based on the comparison.

12. (new) The method as claimed in claim 8, wherein the CPU remains in the separate operating mode by a controller until a second CPU has reached the separate operating mode.

13. (new) The method as claimed in claim 12, wherein the CPU remains in the separate operating mode until the second CPU has reached an end of the separate operating mode.

14. (new) A CPU, comprising:

an execution unit;

a completed instruction counter element for counting a number of instructions executed by the execution unit since a change to a separate operating mode;

a maximum instruction register element that can be specified by an instruction;

a comparator element that compares the maximum instruction register element with the completed instruction counter; and

a cache in the separate operating mode of an external event, the external event retrieved for processing by the CPU while in the separate operating mode.

15. (new) The CPU as claimed in claim 14, wherein the maximum instruction register element has a predetermined value.

16. (new) The CPU as claimed in claim 14, wherein the completed instruction counter element is reset before leaving the separate operating mode.

17. (new) A computer system, comprising:

a first CPU;

a second CPU; and

a connection for a transmission of synchronization information of the separate operating modes between the first and second CPU,

wherein each CPU comprising:

a execution unit,

a completed instruction counter element for counting a number instructions executed by the execution unit since a change to a separate operating mode,

a maximum instruction register element having a predetermined value,

a comparator element that compares the maximum instruction register element with the completed instruction counter, and

a cache in the separate operating mode of an external event, the external event retrieved for processing by the CPU while in the separate operating mode.

18. (new) The computer system as claimed in claim 17, wherein the maximum instruction register element is specified by an instruction.

19. (new) The computer system in claim 17, wherein the completed instruction counter element is reset before the separate operating mode is left.

20. (new) The computer system in claim 17, wherein the first and second CPUs have different clock frequencies.

21. (new) The computer system in claim 17, wherein the first and second CPUs are different CPUs.